SAT-1CS E1/Datacom Tester

SYNERGY TELECOM PVT LTD



Major Features

- © LCD large-screen display, 320×240 lattice, backlight, LED indication
- Hand held, auto configuration
- Multi-task operation at one time
- © Store 20 test results and 9 test configurations, with power-off memories
- Store the test results to PC for analysis and printing
- Automatically power on/off for testing by programmable timer
- Alarm and histogram analysis
- Software updating

Major Functions

Basic functions as below:

- O Normal test
- O Direct connection mode
- Audio frequency test
- O Loop delay test
- Automatic protection switching time testing (APS)
- O Datacom test
- © Co-directional 64 kbit/s test

For 2Mbit/s:

- Service-interrupted error testing
- © Framed and unframed signals generation and reception
- ② 2Mbit/s unframed error performance testing
- © 2Mbit/s framed N×64kbit/s channel error testing
- © Bit error, coding error, frame error, CRC error and E bit error testing

- Signal loss alarm, AIS alarm, framed remote alarm, multi-framed remote alarm, out-of-frame, and pattern loss alarm
- Frequency offset testing
- Line signal level and frequency testing
- O Voice channel signal level and frequency testing
- Pattern slip testing
- Straightforward signaling
- Audio frequency testing
- Coop circuit delay testing
- Automatic protection switching time testing (APS)
- O Voice monitoring
- Signal state display. Voice channel content display. Voice channel busy / idle indication
- Alarm and error histogram analysis
- © Time slot content analysis, drop and insert signal on each time slot
- Framed content analysis
- © G. 821/G. 826/M. 2100 error analysis
- Multi error and alarm inserting
- Three input modes (terminating, bridging and monitoring)
- © Two clock options (internal, external and picking-up)

For Datacom:

- © V.24/RS232/V.28, V.35, V.36, X.21, RS-449, RS-485, RS422, EIA-530, EIA-530A datacom testing
- SYNCH and ASYNCH testing
- DTE and DCE emulation
- Bit code testing
- Pattern slip testing
- © Signal loss alarm
- Line signal level and frequency testing
- O Loop delay testing
- Automatic protection switching time testing(APS)
- © G.821, M2100 service interrupted error testing

For Co-directional 64Kbit/s:

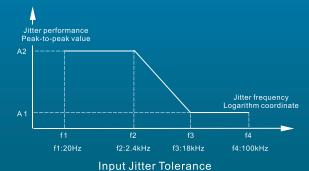
- Service-interrupted
- Bit code testing
- Pattern slip testing
- © Signal loss, AIS alarm
- © Line signal frequency testing
- Coop delay testing
- Automatic protection switching time testing(APS)
- © G.821, M.2100 error testing

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Technical Index

- © 2Mbit/s Technical Index
- (1)Signal input rate: 2048kbit/s ±50ppm (G.703 requirement ±100ppm)
- (2)Signal code: HDB3, AMI.
- (3)Input jitter tolerance: Up to G.823.



(4)Input Impedance

Unbalance terminating: 75Ω G..703 Balance terminating: 120Ω G..703

- (5)Signal structure
 - (5.1) Unframed structure
 - (5.2) Framed structure: PCM30, PCM31, PCM30CRC, PCM31CRC Framed structure complies with the requirement of G. 704
- (6)Testing pattern: 2⁶-1, 2⁹-1, 2¹¹-1, 2¹⁵-1, 2²⁰-1, 2²³-1, and artificial code
- (7)Error code insertion: Bit error, Pattern slip, None single, Ratio 10⁻¹~10⁻⁷.
- © Co-directional 64k Technical Index
 - (1)Signal input rate: 64kbit/s±50ppm(G.703 requirement±100ppm)
 - (2)Input impedance: Balance 120 Ω , up to G.703
 - (3)Input jitter tolerance: Up to G.823.
 - (4)Impedance of output interface: Balance 120Ω , up to G.703
- (5)Testing pattern: 2⁶-1, 2⁹-1, 2¹¹-1, 2¹⁵-1, 2²⁰-1, 2²³-1, and artificial code
- (6)Bit error, pattern slip, none single, ratio, $10^{-1} \sim 10^{-7}$.
- (7) Alarm insertion: None, AIS, Patterless
- O Datacom Technical
 - (1)Data interface type: V.24, V.35, V.36, X.21, RS-449, RS-485, EIA-530 and EIA-530A.
 - (2)Generator
 - (2.1) SYNCH mode

Clock source: Internal and picking-up clock

Phase relation between clock and data: co-direction or reverse direction

Rate: 1.2, 2.4, 4.8, 9.6, 14.4, 19.2, 38.4, 48, 56(kbps), N×64kbps

(N=1~32)

Error: \pm 15ppm (ppm: parts per million)

(2.2) ASYNCH mode

Rate: 50,75,110,150,200,300,600,1200,2400,3600,4800,7200,9600; 14.4k,19.2k,38.4k,57.6k(bps)

Data structure: Word length: 5, 6, 7, 8(bits) Stop bit: 1, 2(bits)

Odd-even check: odd, even, 1, 0, none

(2.3) Error code insertion: None, single, or ratio 10⁻¹~10⁻⁷.

(3)Receiver

(3.1) SYNCH mode

Clock source: Internal and picking up clock

Phase relation between receive clock and receive data: Co-direction or reverse direction.

Clock Rate: 2048kbps at a maximum

(3.2) ASYNCH mode

The rate and data structure are the same as the generator.

(4)Testing pattern: 2⁶-1, 2⁹-1, 2¹¹-1, 2¹⁵-1, 2²⁰-1, 2²³-1, and artificial code

Other Parameters

- O Power supply
 - (1)Special power adapter

Input: AC220V 50Hz

Output: DC 9V 1.2A

(2)Internal rechargeable battery

4000mAh, 6V nickel-hydrogen rechargeable battery

Working time: 8 hours

Charging: 8 hours at power-off state, and 12 hours at power-on state

O Dimension and weight

L×W×H: 220×162×48mm

Weight: 0.95kg

Ambient parameters

